We Claim:

1. A multilevel FLASH cell architecture comprising:

at least one FLASH cell;

a plurality of reference generators;

a plurality of comparators coupled to the FLASH cell via a sensing node and coupled to the plurality of reference generators; the plurality of comparators for comparing a signal of the sensing node to a full spectrum of reference voltage signals in parallel from the plurality of reference generators; and providing outputs; and

translation logic coupled to the plurality of comparators for decoding the outputs to determine the state of the FLASH cell.

2. The FLASH cell architecture of claim 1 wherein the most significant bit (MSB) and the least significant bit (LSB) of the state is provided from the translation logic.

3. The FLASH cell architecture of claim 2 wherein the translation logic detects underprogramming and overprogramming of a FLASH cell by comparing the sensing node to limits for each state.

4. The FLASH cell architecture of claim 2 wherein the translation logic detects when the cell is properly programmed.

5. The FLASH cell architecture of claim 2 wherein the translation logic detects if the current state of the FLASH cell matches the desired data to indicate successful data validation.

6. The FLASH cell architecture of claim 2 wherein if the translation logic detects that the current state of the FLASH cell is less than the desired state further programming is necessary to provide the data within the desired state limits.

7. The FLASH cell architecture of claim 2 wherein if the translator logic detects that the cell is overprogrammed an error signal is detected.

8. The FLASH cell architecture of claim 1 wherein the full spectrum of reference signals include boundary reference voltages between states and upper and lower target voltages within a state.

9. The FLASH cell architecture of claim 1 wherein the plurality of reference generators are coupled together such that a first reference generator provides a base current and subsequent reference generators add sequentially increasing amount of delta current to the lease current.

10. The FLASH cell architecture of claim 9 wherein a margin between reference generators is adjusted by arbitration codes that select currents for summing.

11. The FLASH cell architecture of claim 1 wherein each reference voltage generator generates a current for each boundary between 2^n states and for an upper limit and a lower limit for each state.

12. The FLASH cell architecture of claim 1 which includes a control engine for decoding received addresses wherein the row address causes a row of cells to be activated and a column address activates the reference generators and a multichannel cell address.

13. The FLASH cell architecture of claim 1 wherein the at least one FLASH cell comprises a memory cell array.

14. The FLASH cell architecture of claim 13 wherein there are multi-level states per cell.

15. The FLASH cell architecture of claim 13 which includes an I/O buffer coupled to the translation logic.

16. The FLASH cell architecture of claim 15 which includes a write/cache buffer coupled to the translation logic.

17. The FLASH cell architecture of claim 16 which includes a fast one stage read/write control engine with progressive state indicators coupled to translation logic.

18. The FLASH cell architecture of claim 17 which includes a set of external and auto calibration registers coupled to the control engine.

19. The FLASH cell architecture of claim 18 which includes a set of reference calibration commands in addition to the read, erase and program commands.

20. The FLASH cell architecture of claim 19 which includes a voltage/current reference generator coupled to the FLASH cell memory array and the calibration registers.

21. The FLASH cell architecture of claim 20 which includes a plurality of address registers coupled to a row address decoder and a calendar address decoder.

22. The FLASH memory device of claim 13, further comprising:

a plurality of memory cell strings each connected to x-y addressable word lines and bit lines.